

MIMXRT1060-EVKB

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1. Unless Otherwise Specified:
- All resistors are in ohms, 1/16 Watt,0402
 - All capacitors are in uF,0402
 - All voltages are DC
 - All polarized capacitors are aluminum electrolytic
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

Revision History

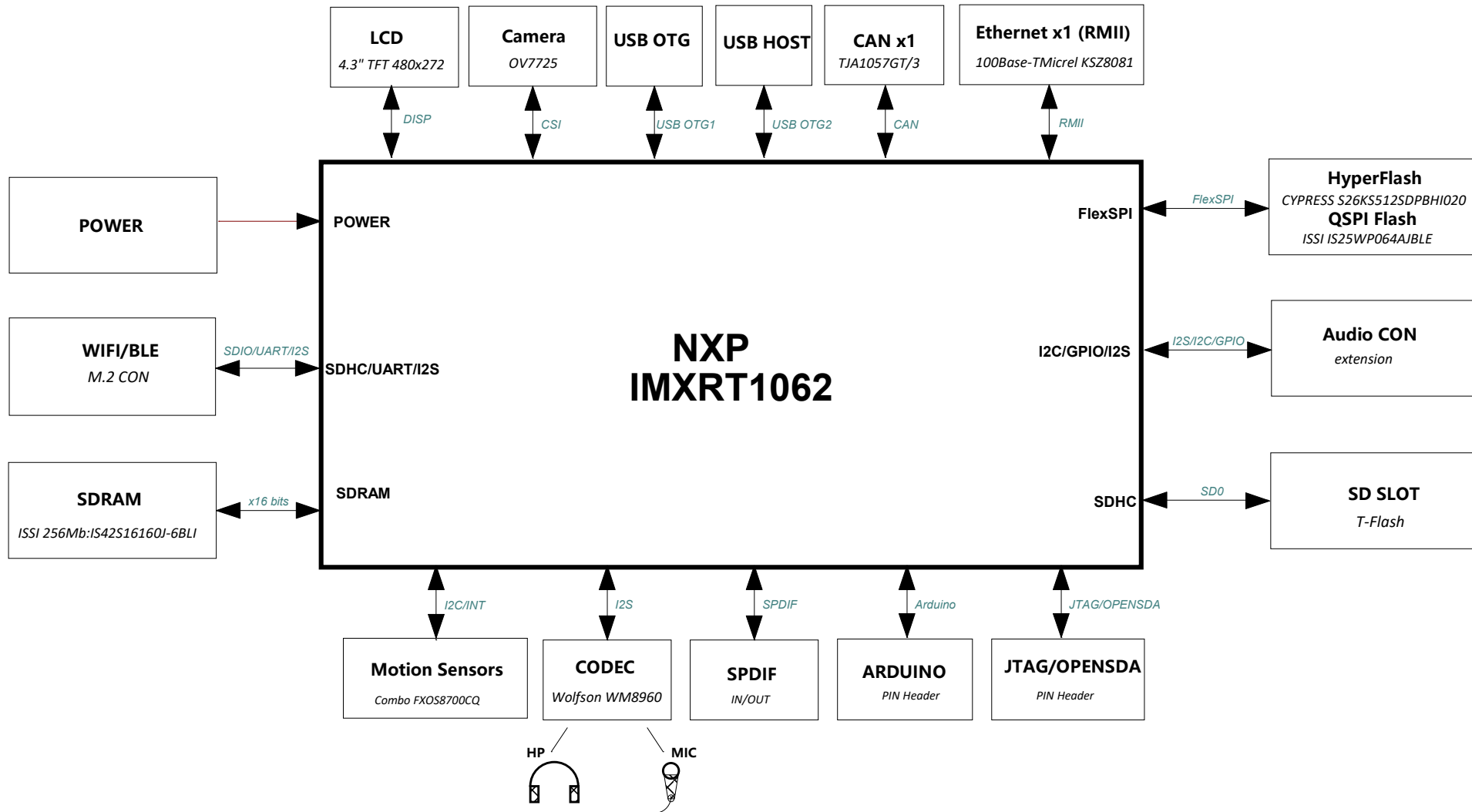
Rev. Code	Date	By	Description																								
A	2020-11-27	Shawn Shi	Initial Release																								
B	2021-03-17	Shawn Shi	1.Add R432,R433 for SD power switch 2.Change R232 from 10K to 100K 3.Swap I2C3_SCL and I2C3_SDA 4.Add R434,R435 for I2C signal pull-up 5.DNP R252, R345.Populate R160,R162,R164,R167,R176,R382,R390,R396,R415																								
B1	2021-06-03	Albert Li	No Layout change compared to RevB, only BOM update: 1.DNP R368,R376,R347,R349,R365,R363 2.Add note in page05 to populate resistors for M.2 SDIO App.																								
			<table><tr><th>REF DES</th><th>JUMPER(DEFAULT)</th><th>PAGE NAME</th></tr><tr><td>J40</td><td>5-6</td><td>03 MAIN POWER</td></tr><tr><td>J44,J29,J27,J25,J30,J26</td><td>1-2</td><td>04 POWER DOMAIN</td></tr><tr><td>J41,J35,J37,J36</td><td>1-2</td><td>09 AUDIO</td></tr><tr><td>J5,J6,J13,J9,J11,J3,J10,J4</td><td>1-2</td><td>15 FREELINK</td></tr></table> <table><tr><th>REF DES</th><th>SWITCH(DEFAULT)</th><th>PAGE NAME</th></tr><tr><td>SW3,SW2</td><td>off,off,off,off</td><td>17 BOOT</td></tr><tr><td>SW4</td><td>off,off,on,off</td><td>17 BOOT</td></tr></table>	REF DES	JUMPER(DEFAULT)	PAGE NAME	J40	5-6	03 MAIN POWER	J44,J29,J27,J25,J30,J26	1-2	04 POWER DOMAIN	J41,J35,J37,J36	1-2	09 AUDIO	J5,J6,J13,J9,J11,J3,J10,J4	1-2	15 FREELINK	REF DES	SWITCH(DEFAULT)	PAGE NAME	SW3,SW2	off,off,off,off	17 BOOT	SW4	off,off,on,off	17 BOOT
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SW4	off,off,on,off	17 BOOT																									

3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
- _B Denotes - Active-Low Signal
 - <> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

		Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78755-6590	
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ICAP Classification: CP:		IUC:	PUBL:
Designer: Shawn Shi	Drawing Title: MIMXRT1060-EVKB		
Drawn by: Shawn Shi	Page Title: COVER		
Approved: Yes	Size C	Document Number SCH-47858, PDF: SPF-47858	Rev B1
Date: Thursday, June 03, 2021		Sheet 1	of 18

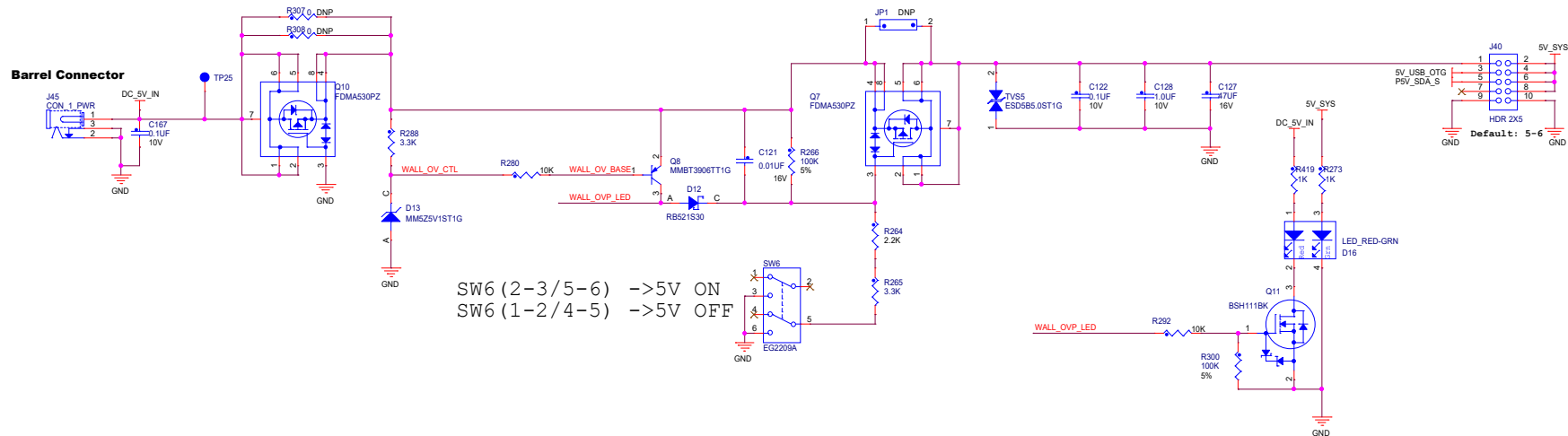
Blcok Diagram Rev B#####

MIMXRT1060-EVKB

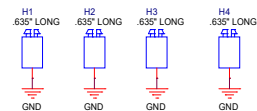


ICAP Classification: CP: _____ IUC: X PUB: _____			
Drawing Title: MIMXRT1060-EVKB			
Page Title: BLOCK DIAGRAM			
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Main Power



Board Mounting Holes

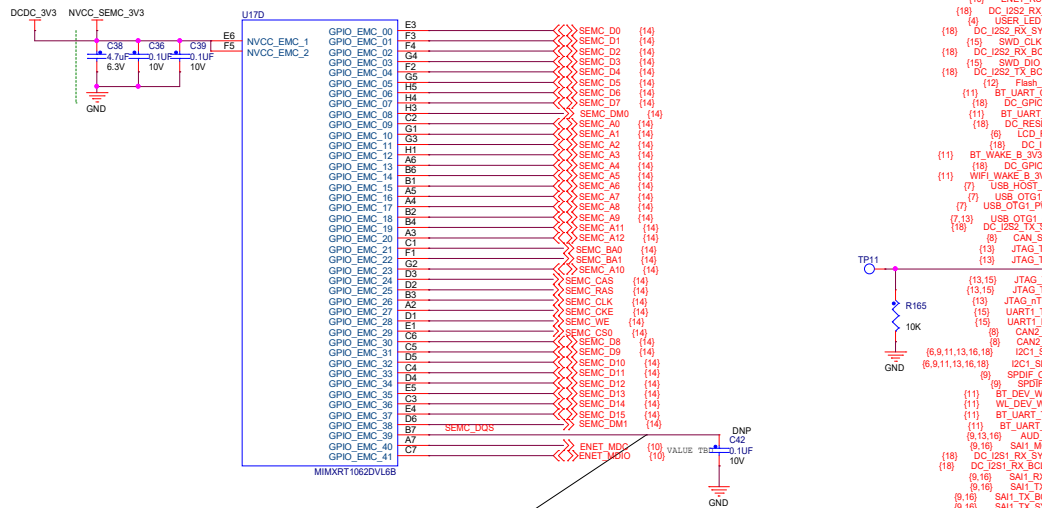


Ground TPs



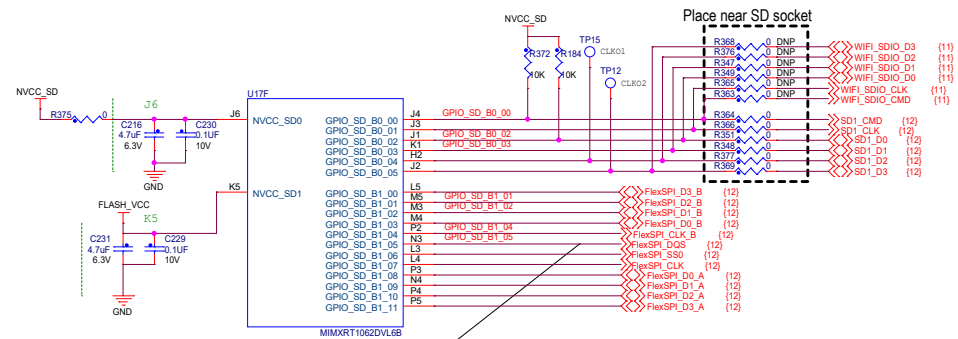
Layout Note: Place Ground TPs to assist signal measurement.

ICAP Classification: CP: IUX: X PUB:			
Drawing Title: MIMXRT1060-EVKB			
Page Title: MAIN POWER			
Size C	Document Number SCH-47858, PDF: SPF-47858	Rev B1	
Date: Thursday, June 03, 2021	Sheet 3 of 18		

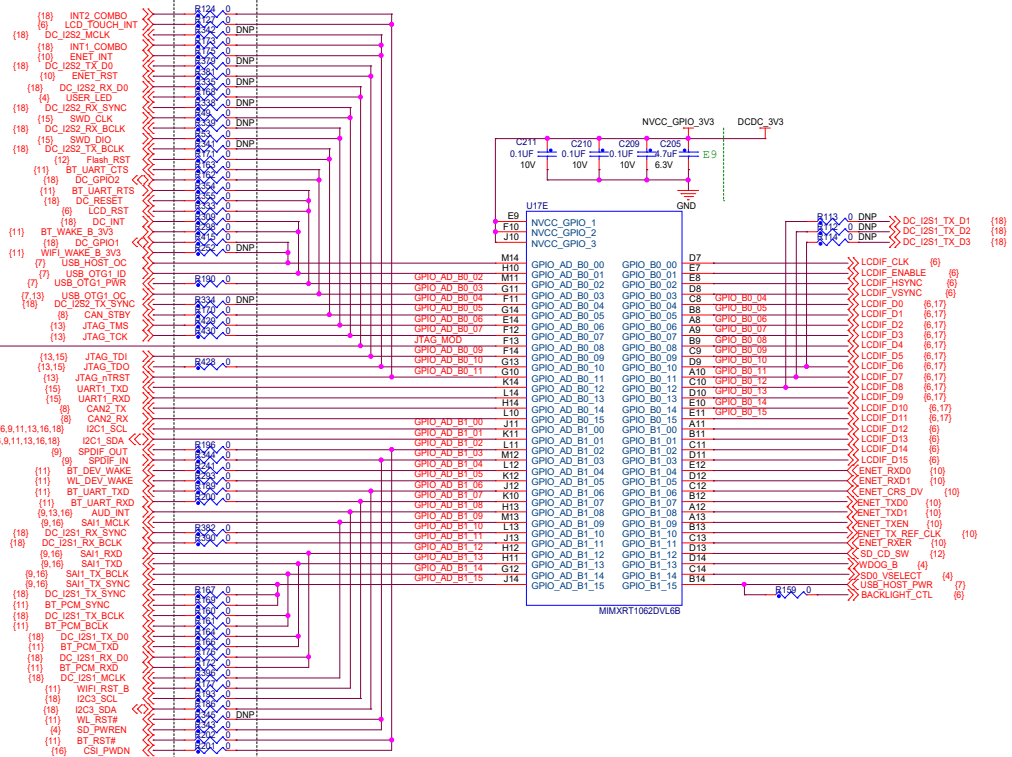


SEMC DQS PIN need floating for SDRAM RW @166MHz

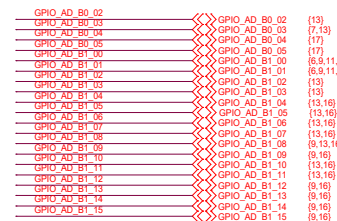
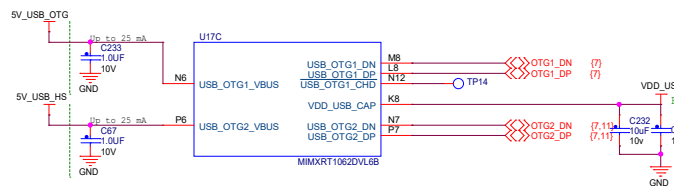
Note: Populate R368,R376,R347,R349,R365,R363 when run M.2 SDIO related examples.



FlexSPI DQS PIN need floating for QSPI Flash RW @133MHz



Those 0ohm resistors are used for signal mutlplexion usage, should avoid long stub in layout for signal integrity



Up to 150 mA @5V

5V_SYS

R156 0

C45 7µF 6.3V

C43 0.1µF 10V

U14

L3 100µF

D7 MBRA160T3G

C41 2µF 35V

R145 0

BL+

BL-

VREF=200mV, DRIVE CURRENT 40mA

(5) Backlight_CTL

R144 100K

R136 10

R137 10

C37 0.1µF 10V

UM1661

Up to 12.5 mA @3.3V

PERI_3V3

LCD_3V3

R336

C191 4.7uF 6.3V

C189 10uF 10V

C190 10uF 10V

GND

(5,17) LCDIF_D11

(5) LCDIF_D12

(5) LCDIF_D13

(5) LCDIF_D14

(5) LCDIF_D15

(5,17) LCDIF_D5

(5,17) LCDIF_D6

(5,17) LCDIF_D7

(5,17) LCDIF_D8

(5,17) LCDIF_D9

(5,17) LCDIF_D10

(5,17) LCDIF_D0

(5,17) LCDIF_D1

(5,17) LCDIF_D2

(5,17) LCDIF_D3

(5,17) LCDIF_D4

(5) LCDIF_CLK

(5) LCDIF_HSYNC

(5) LCDIF_VSYNC

(5) LCDIF_ENABLE

LCD_3V3

R337

10K

GND

C192 10uF 10V

(5,11,13,16,18) LCD_RST

(5,11,13,16,18) I2C1_SCL

(5,11,13,16,18) I2C1_SDA

GND

B1

B2

RESET

INT

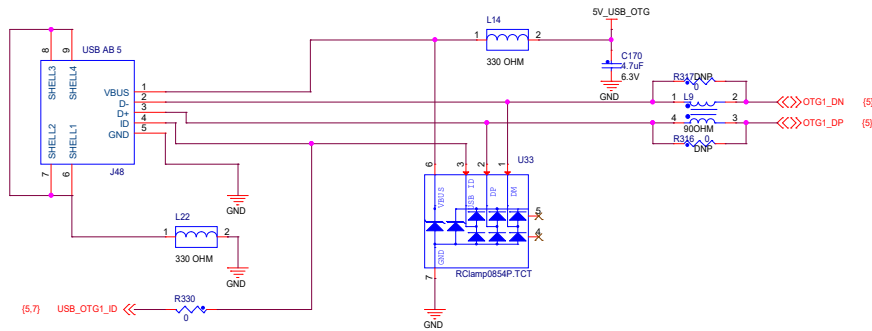
SCL

SDA

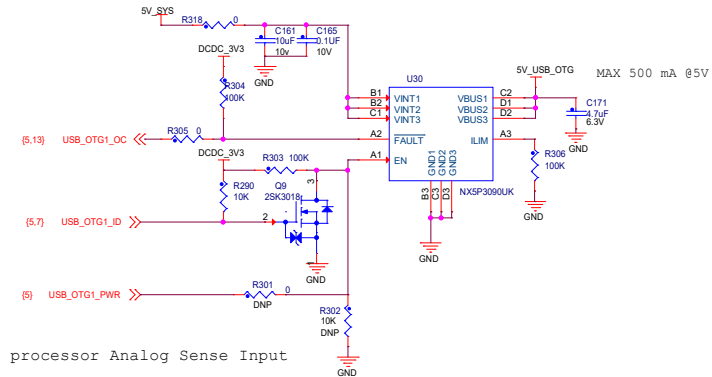
GND1

CON 1X40 + CON 1X6 + TFT DISPLAY

USB OTG



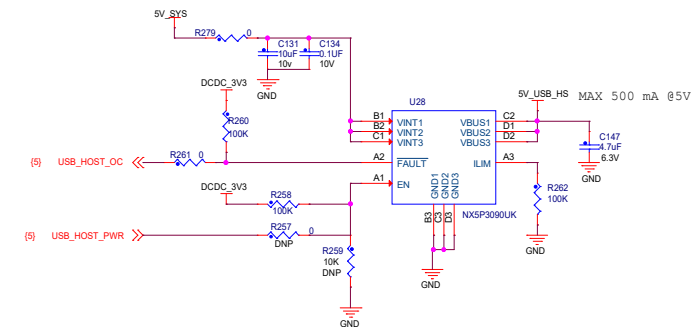
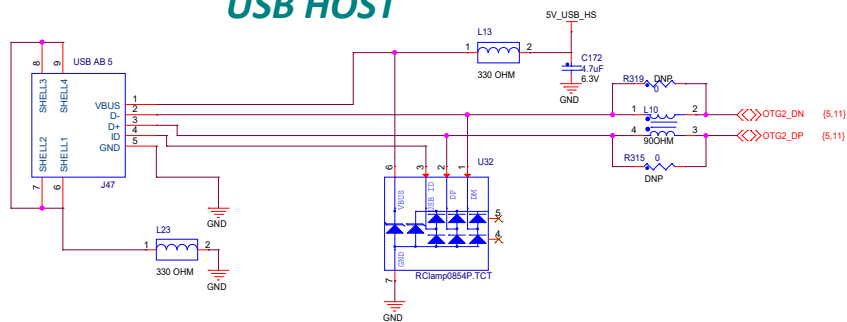
USB POWER



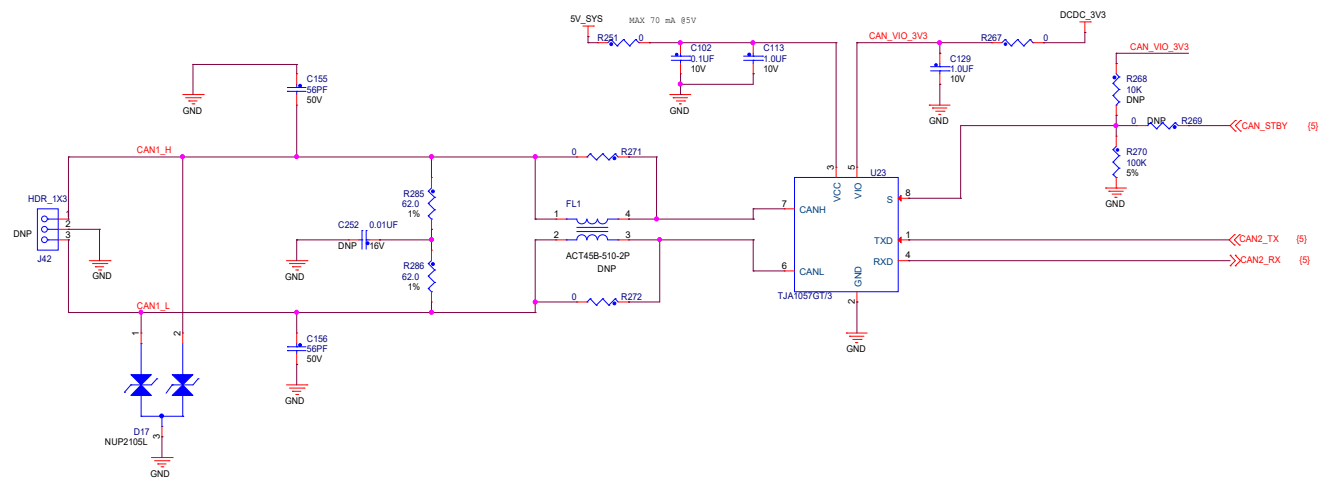
USB ID is a processor Analog Sense Input

Host --> ID = GND
Device --> ID = Floating

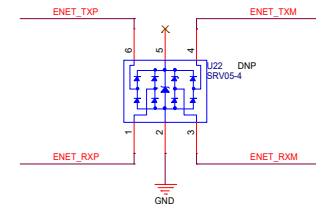
USB HOST



CAN BUS



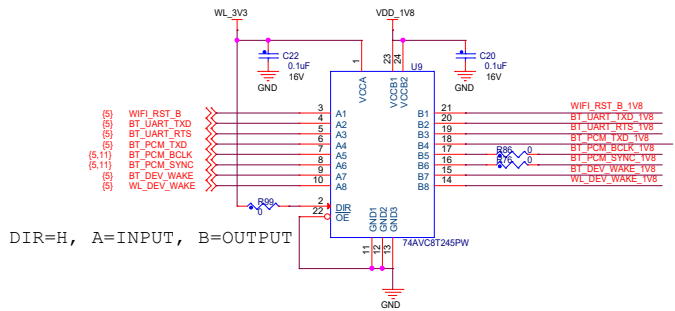
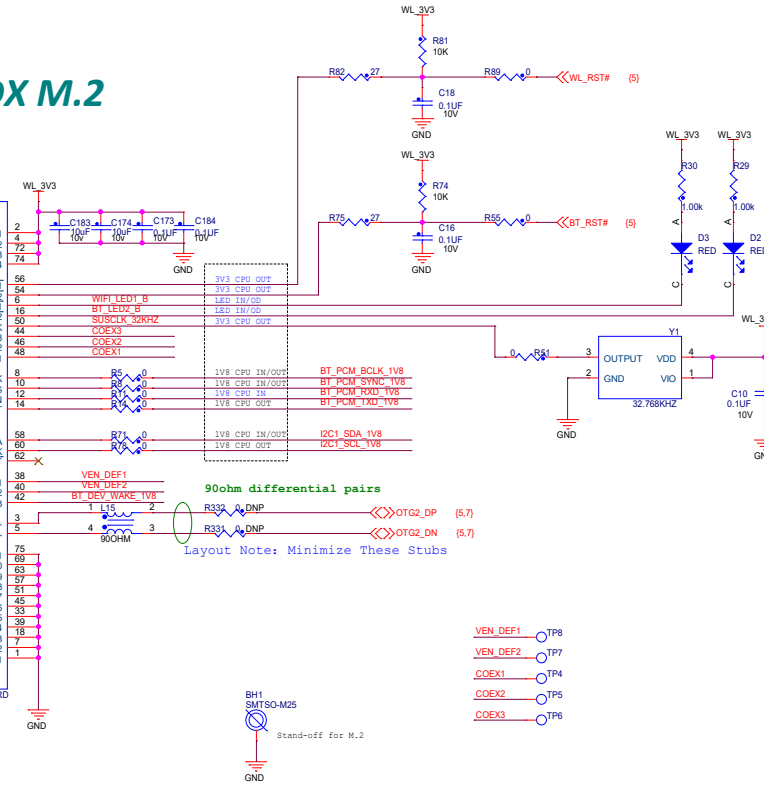
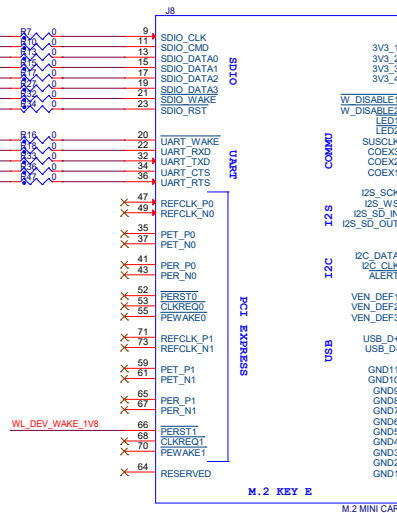
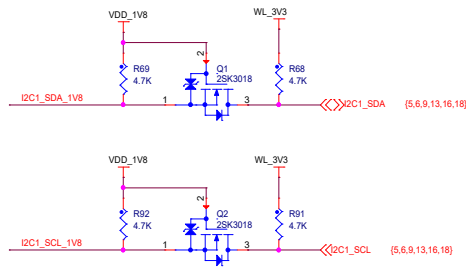
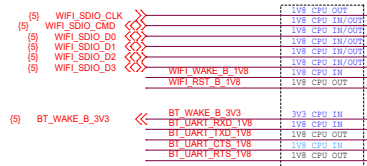
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CAN				
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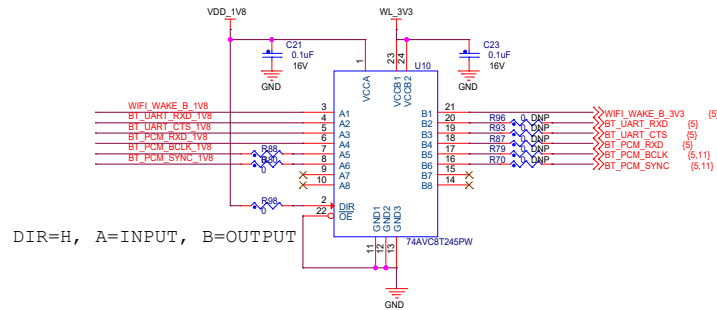


Compatible with 1DX M.2

To apply M.2 based card, need put on J8 to switch SDIO signals as 1.8V



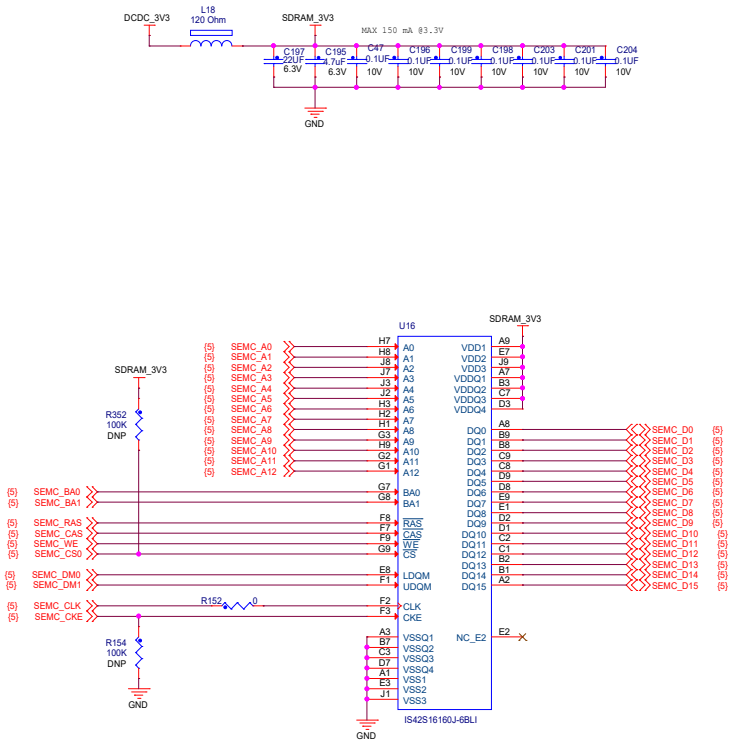
DIR=H, A=INPUT, B=OUTPUT



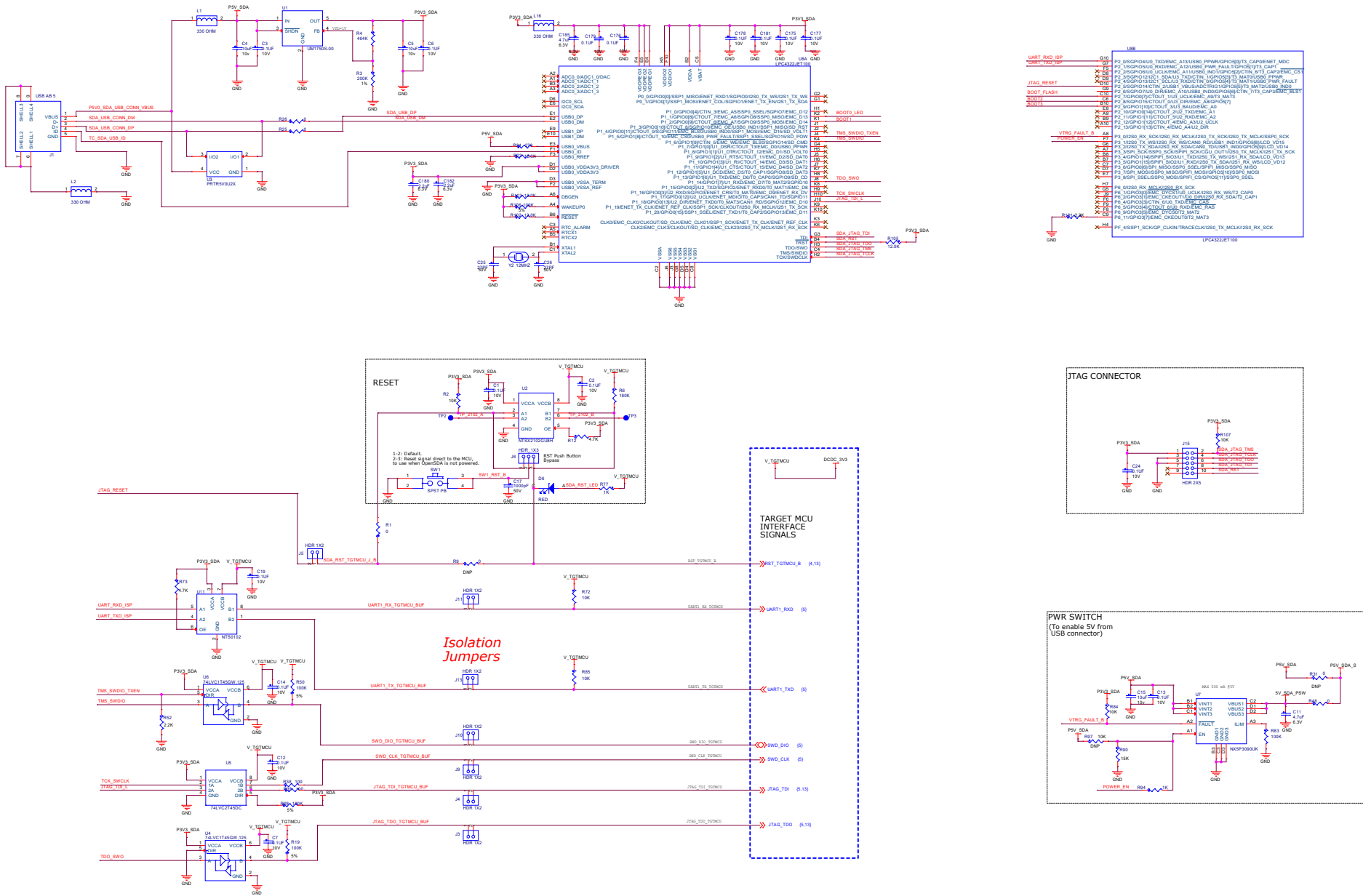
DIR=H, A=INPUT, B=OUTPUT



SDRAM

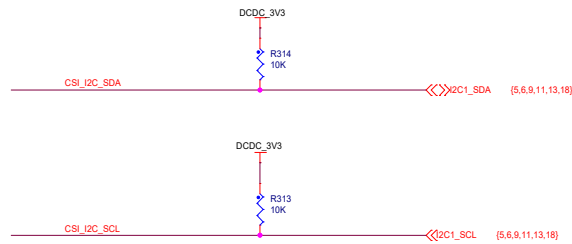
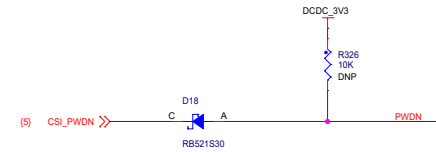


Freelink Interface

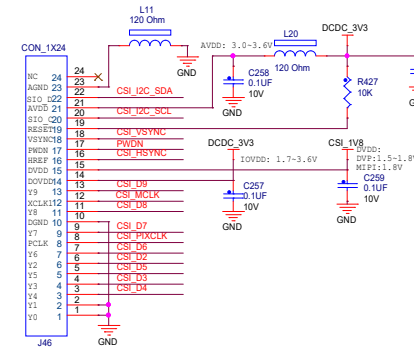


Camera Signals

CSI_PIXCLK	R321	0	GPIO_AD_B1_04	(5,13)
CSI_MCLK	R320	0	GPIO_AD_B1_06	(5,13)
CSI_VSYNC	R327	0	GPIO_AD_B1_06	(5,13)
CSI_HSYNC	R325	0	GPIO_AD_B1_07	(5,13)
CSI_D0	R324	0	GPIO_AD_B1_08	(5,9,13)
CSI_D8	R426	0	GPIO_AD_B1_09	(5,9)
CSI_D7	R322	0	GPIO_AD_B1_10	(5,13)
CSI_D6	R320	0	GPIO_AD_B1_11	(5,13)
CSI_D5	R425	0	GPIO_AD_B1_12	(5,9)
CSI_D4	R424	0	GPIO_AD_B1_13	(5,9)
CSI_D3	R423	0	GPIO_AD_B1_14	(5,9)
CSI_D2	R422	0	GPIO_AD_B1_15	(5,9)

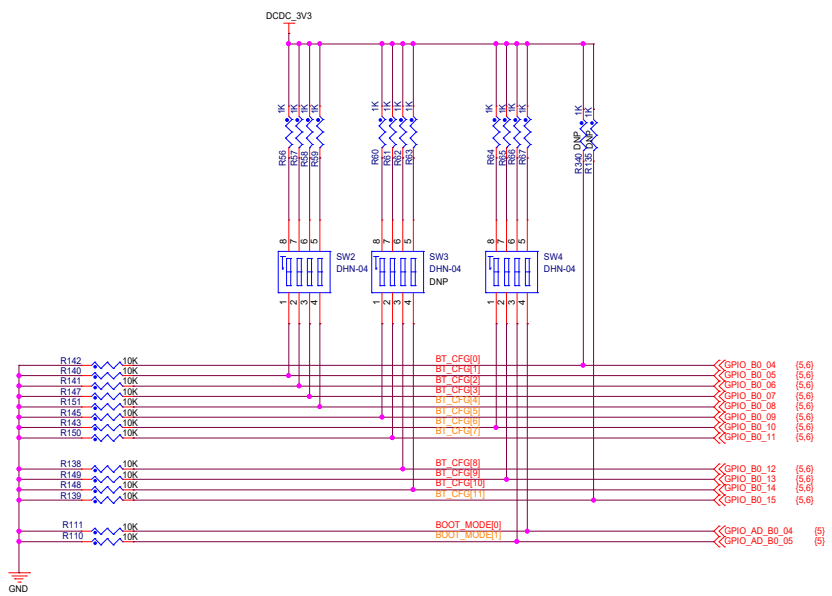


FPC FOR MT9M114/OV7725 MODULE



BOOT CONFIG TABLE

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
FlexSPI - Serial NOR	Infinit-Loop: (Debug USE only) 0 - Disable 1 - Enable	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			0	0	0	0	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		EncryptedXIP 0 - Disabled 1 - Enabled	Reserved
SD	Infinit-Loop: (Debug USE only) 0 - Disable 1 - Enable	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Fast Boot: 0 - Regular 1 - Fast Boot



COMBO SENSOR


FXOS8700CQ COMBO SENSOR

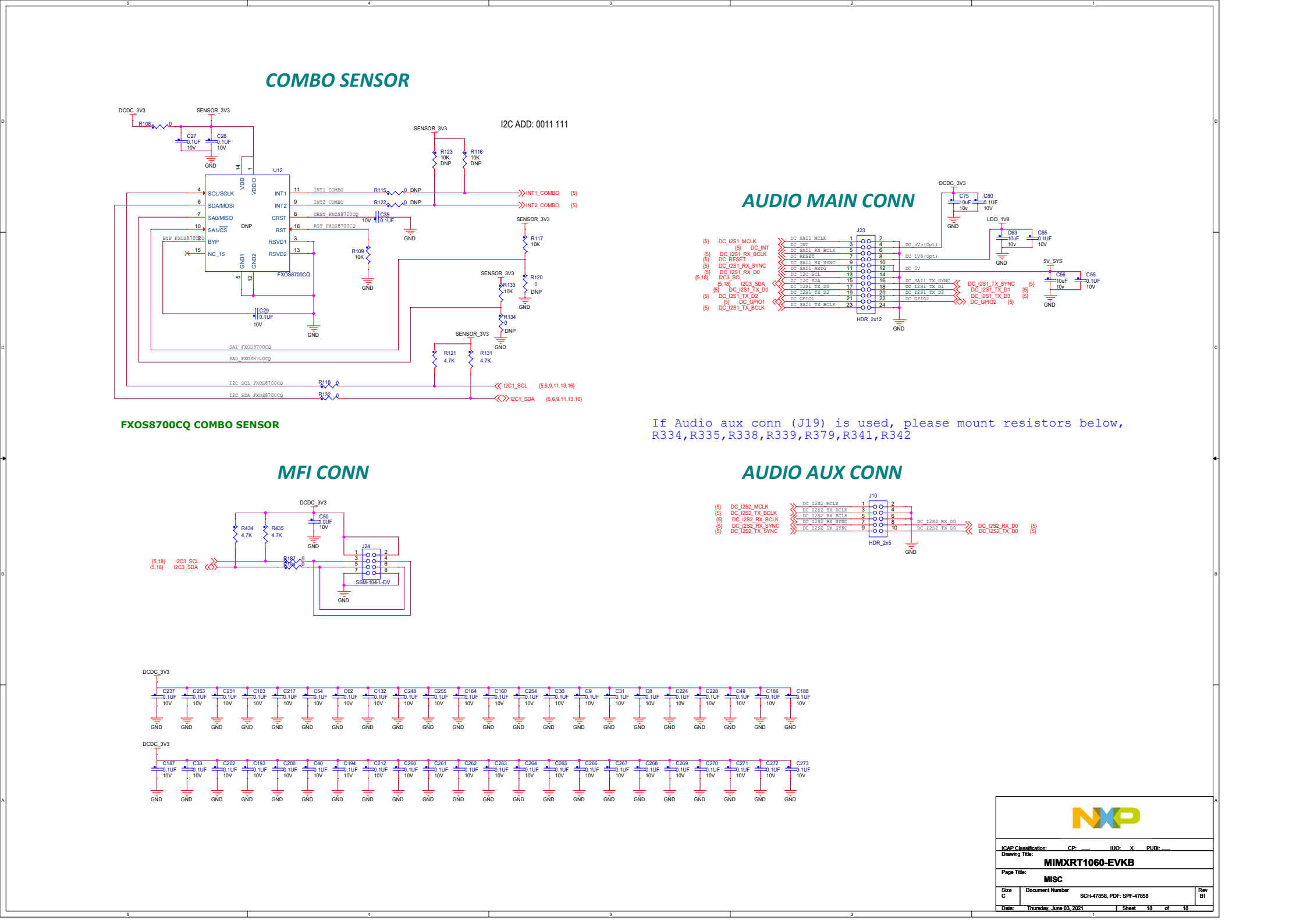
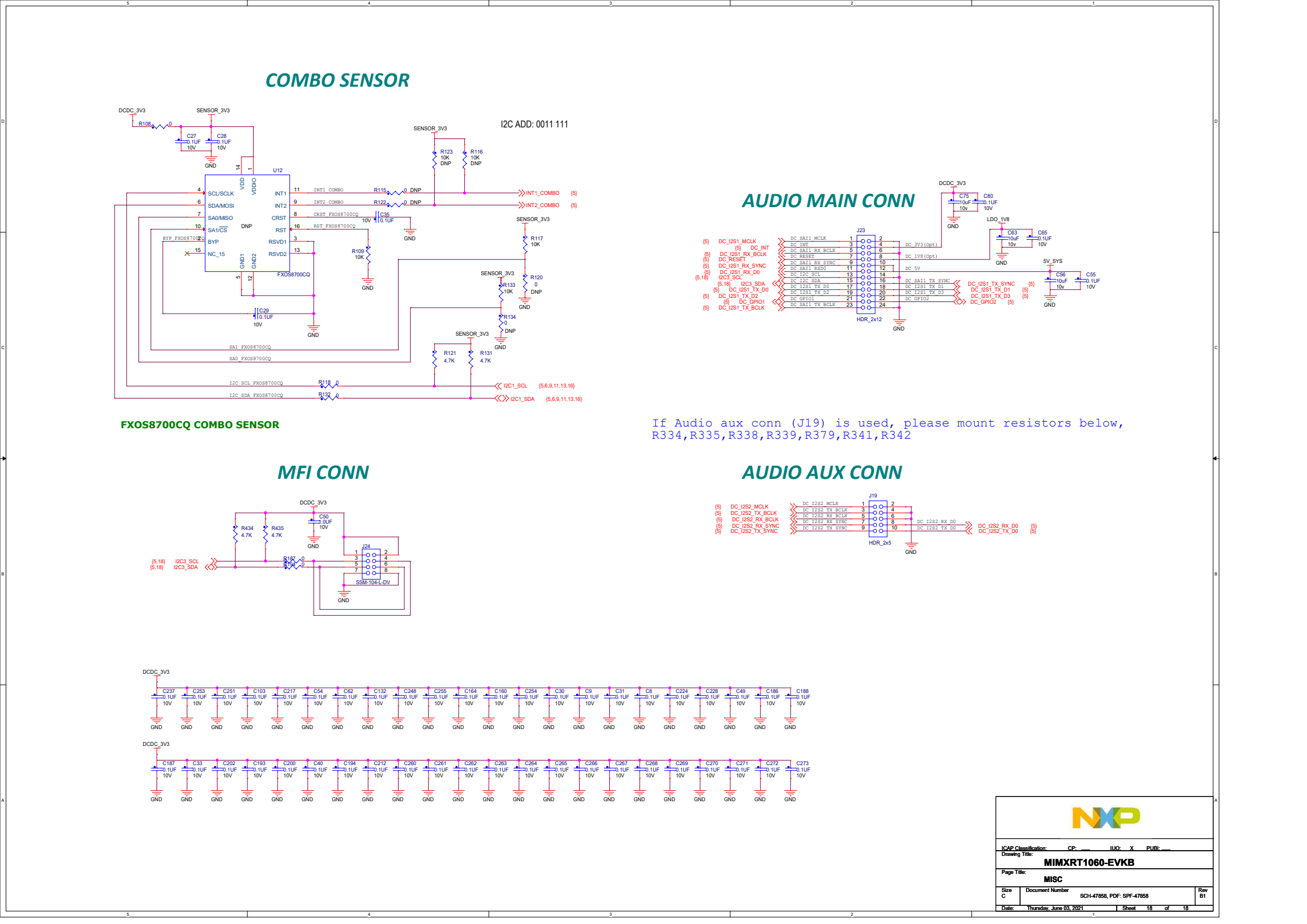
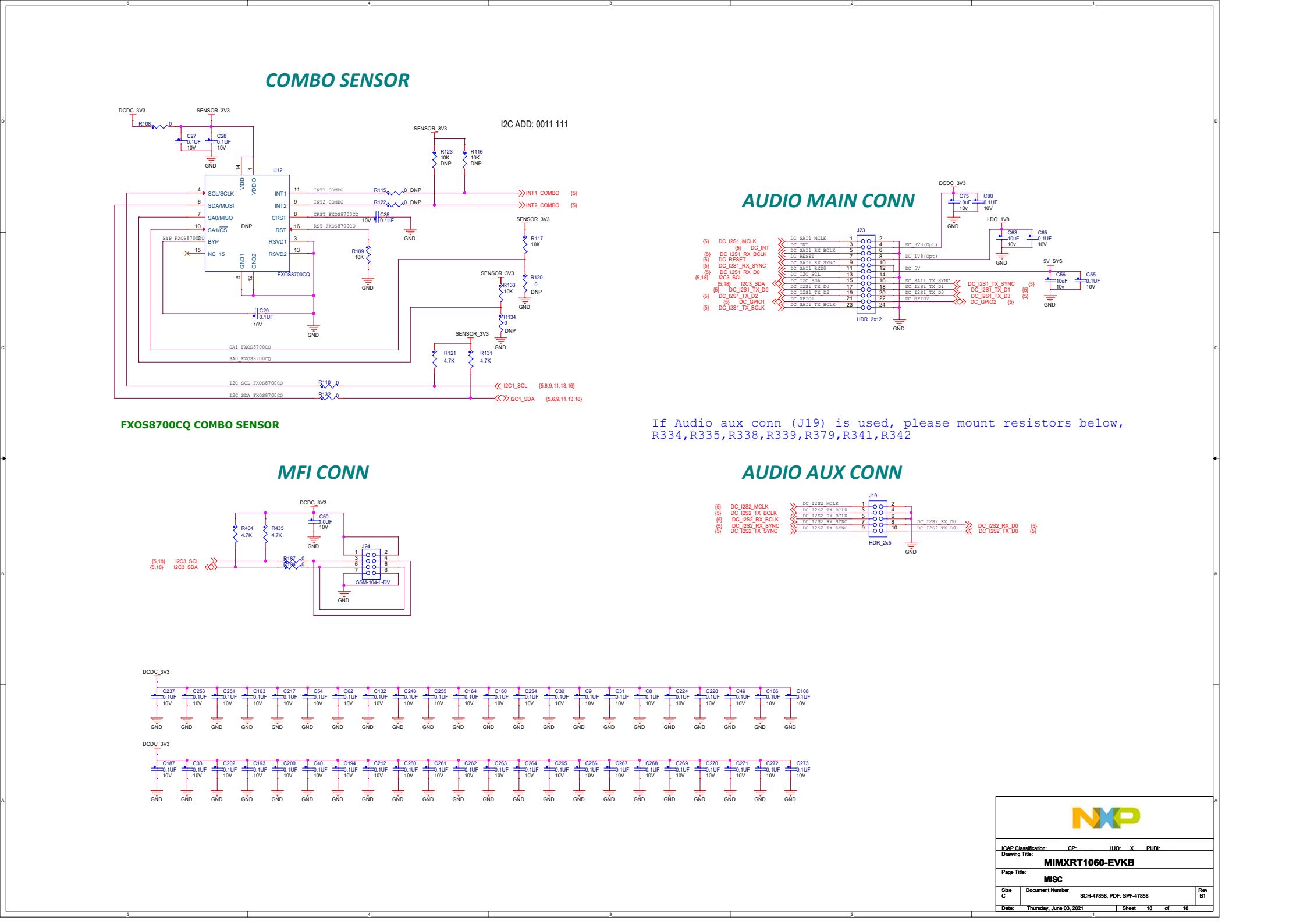
MFI CONN

AUDIO MAIN CONN

If Audio aux conn (J19) is used, please mount resistors below, R334,R335,R338,R339,R379,R341,R342

AUDIO AUX CONN

			
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MISC			
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